AlGaN/GaN/AlN quantum-well field-effect transistors with highly resistive AlN epilayers

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AlGaN/GaN/AlN quantum-well field-effect transistors have been demonstrated. By replacing a semi-insulating GaN epilayer with a highly resistive AlN epilayer in the device structure, parasitic conduction in the GaN epilayer, leakage current through the GaN epilayer, and the channel electrons spillover into the GaN epilayer have been completely eliminated and the drain current collapse has been reduced. The fabricated devices on sapphire substrate with 1 μm gate length show a high saturation current (>1 A/mm), and excellent gate control capability with a pinch-off voltage of −6 V. Even without passivation, the devices exhibit small drain current collapse (<10%) under 1 μs pulse gate driving. © *2006 American Institute of Physics*. [DOI: 10.1063/1.2174847]

AlGaN/GaN heterostructure field-effect transistors (HFETs) have reached a very high-performance level. However, they still suffer from serious reliability and stability problems. The conventional AlGaN/GaN HFET structure is generally formed by depositing a layer of AlGaN on a relatively thick semi-insulating GaN epilayer. Since it is very challenging to produce semi-insulating GaN epilayers with high resistivity, many of the problems are caused by the use of the thick semi-insulating GaN epilayer in the device structure. The current collapse phenomenon under radio-frequency operation,[1] which has been attributed to the surface charge[2] and charge trapping in the GaN bulk,[3] limits the output microwave power. The low resistance of the GaN bulk layer introduces a parasitic current, which degrades the device performance and, in the worst case, does not allow the transistor to be pinched off. Although growth at low pressure by introducing more defects[4] or antidoping by carbon[5] or iron[6] may be used to increase the resistivity of GaN, the dopants also increase the defects density in the GaN bulk, which was shown to further enhance the current collapse effect.[4]

Since AlN with a band gap of 6.1 eV is highly resistive, and high-quality AlN epilayers can be grown[7,8] and bulk AlN substrates are also available,[9] an interesting question arises as to whether we substitute the GaN bulk layer with highly resistive AlN bulk layer to build AlGaN/GaN/AlN quantum-well field-effect transistor (QW-FET) devices, in which the parasitic conduction in the bulk is completely eliminated. Considering the large conduction-band edge discontinuity between AlN and GaN, the incorporation of a thick underneath AlN epilayer, in principle, can provide an effective confinement that limits the electron spillover into the bulk, resulting in a reduction of the output conductance. This confinement effect and the highly resistive nature of AlN should also diminish the current collapse related with the bulk trapping, and reduce the leakage current. The quantum-well confinement may also have the benefit of improving the high-frequency response of the device. It should be pointed out that the QW-FET we are proposing here, as shown schematically in Fig. 1(a), has a very thin GaN channel layer, which is different from the typical AlGaN/GaN HFET grown on AlN/sapphire or an AlN/SiC template.[10]

Unfortunately, the large spontaneous and strain-induced polarization effects, which are very unique to nitride semiconductors, might cause a serious problem to this AlGaN/GaN/AlN QW-FET structure, since the negative po-

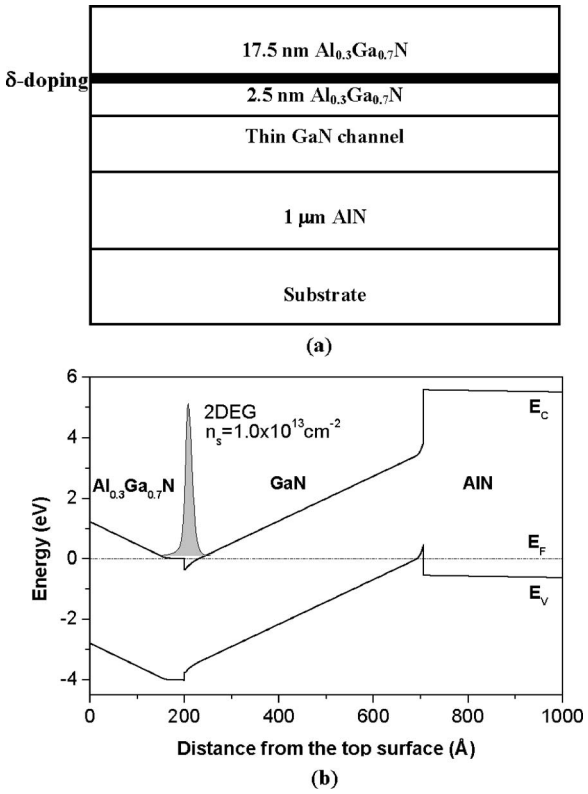

FIG. 1. The schematic diagram (a) and the simulated band diagram (b) of the AlGaN/GaN/AlN QW-FET structure used in this study. A Si δ-doping level of 4.5×10^{12} cm^{-2} and 50 nm GaN layer thickness are used for the calculation.

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larization charge at the bottom GaN/AlN interface could possibly deplete the two-dimensional electron gas (2DEG), which, on the other hand, is enhanced by this same polarization effect at the top AlGaN/GaN interface. Our numerical simulation and experimental results show that this problem can be overcome by band-engineering and suitable doping scheme, so that the highly resistive AlN layer can be employed to design an AlGaN/GaN/AlN QW-FET structure. Guided by simulation results, we have successfully grown the layer structure and fabricated AlGaN/GaN/AlN QW-FET devices with a very high-level of dc performance and small current collapse under pulse gate driving, which demonstrates the excellence of this unique structure.

The energy band and the electron distribution of the AlGaN/GaN/AlN structure are calculated by solving both Poisson equation and Schrödinger equation self-consistently.[11,12] We assume that all layers have the Ga (or Al) crystal face. The data from the literature[13,14] on the spontaneous and piezoelectric induced charges are incorporated in the calculation. Specifically, the spontaneous polarization-induced surface charge densities for relaxed AlN and GaN, respectively, are 5.62×10^{13} and 2.12×10^{13} cm^{-2}, and the bound interface charge density of pseudomorphic $Al_{0.3}Ga_{0.7}N$/GaN on relaxed GaN is estimated to be 1.5×10^{13} cm^{-2}. The conduction-band offsets of $Al_{0.3}Ga_{0.7}N$/GaN and GaN/AlN are 0.35 and 1.71 eV, respectively. For the boundary conditions, the top surface energy level is pinned by the Ni Schottky gate at 1.23 eV for $Al_{0.3}Ga_{0.7}N$, and the Fermi level at the bottom interface is assumed at the midgap of the thick AlN layer.[14] Our previous experimental work[15] has demonstrated that the conventional AlGaN/GaN HFET grown on GaN layer with the δ-doping scheme has a better performance than uniform doping. This conclusion is consistent with the present calculation, which shows that in the conventional AlGaN/GaN HFET structure, under the condition of the same amount of silicon dopants, the 2DEG density n_s in the channel increases 14% by δ-doping over the uniform doping. This improvement is not surprising, considering that uniformly distributed silicon ions will screen the polarization field. In this work, we retain the δ-doping scheme in the top AlGaN barrier layer. The calculated band diagram for the AlGaN/GaN/AlN QW-FET structure shown in Fig. 1(a) is depicted in Fig. 1(b). The GaN channel layer with a thickness of 50 nm, which is much larger than the critical thickness of GaN/AlN heterostructure, is treated as fully relaxed, and only spontaneous polarization charges appear at the GaN/AlN interface. Since an electrical field should not exist in the bulk AlN, we assume there exist n-type donors with a density of 5×10^{16} cm^{-3} on the top 200 nm of AlN (near the GaN/AlN interface). Our simulation demonstrates that these donors in AlN only modify the electrical field in the bulk AlN, but has no influence on the 2DEG density, n_s, in the channel. It is clear from Fig. 1(b) that the negative bounded charge at the GaN/AlN interface will deplete the electrons in the GaN channel by lifting up the conduction-band edge. Compared to the n_s value in the conventional AlGaN/GaN HFET structure, our simulation results indicate that the n_s value in the unoptimized AlGaN/GaN(50 nm)/AlN QW-FET structure is about 30% lower [see Fig. 2(b)], which is clearly not acceptable.

In order to take the advantage of the AlN epilayer, and at the same time without sacrificing the high n_s, the AlGaN/GaN/AlN QW-FET structure has to be optimized.

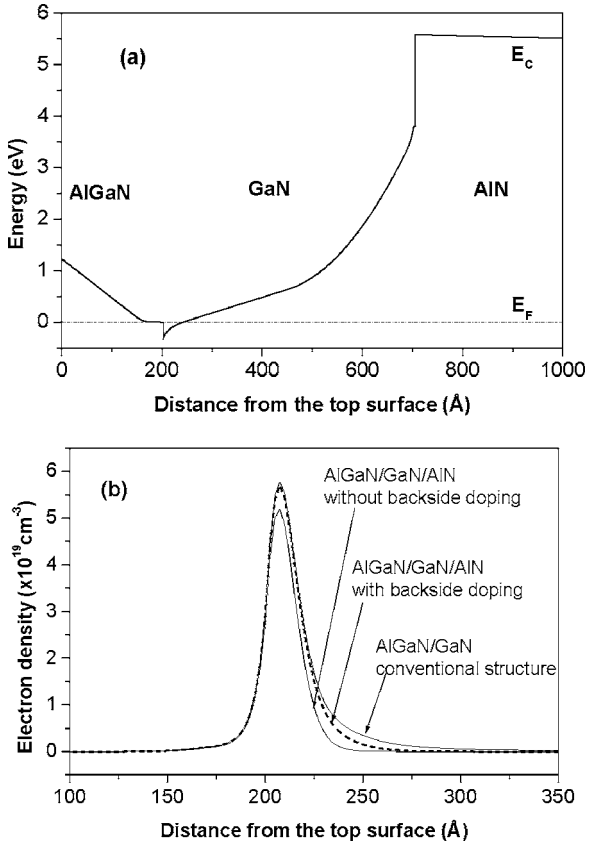

FIG. 2. (a) The simulated conduction-band edge of AlGaN/GaN/AlN QW-FET structure with back side doping. For the total 50 nm GaN layer thickness, the bottom 25 nm is doped with silicon (4×10^{18} cm^{-3}). (b) Comparison of the electron distributions with and without back side doping. The electron distribution for the conventional AlGaN/GaN HFET structure is also included. With back side doping, AlGaN/GaN(50 nm)/AlN QW-FET structure has the similar sheet electron density as the conventional structure.

One might expect that the depletion effect by the negative polarization charge at the GaN/AlN interface will be reduced as we separate the two interfaces further away by increasing GaN layer thickness.

Another option to achieve high n_s is back side doping. In a previous work, graded AlGaN was employed for back doping.[16] From Fig. 1(b), we notice that the polarization charges at the GaN/AlN interface lift up the band edge of GaN and introduce a built-in electrical field, pointing to the two-dimensional (2D) channel at the AlGaN/GaN interface. If we dope the bottom side of GaN layer, the introduced electrons will accumulate in the 2D channel naturally, separating from the dopant atoms by this field. Figure 2 shows the simulated conduction-band edge and electron distribution for one case of back side doping. In this case, the total thickness of GaN layer is 50 nm, while the bottom 25 nm is doped by silicon with a dopant density of 4×10^{18} cm^{-3}. As expected, electrons introduced by back side doping accumulate in the 2D channel, and the 2DEG density reaches a level (1.4×10^{13} cm^{-3}) that is comparable to that in a conventional AlGaN/GaN heterostructure.

Next, we present some initial results of our fabricated devices. Guided by the simulation studies, we grew AlGaN/GaN(50 nm)/AlN QW-FET structure on sapphire by metalorganic chemical vapor deposition and the device structure is schematically shown in Fig. 1(a). In the device, we incorporated 1 μm thick highly resistive AlN epilayer

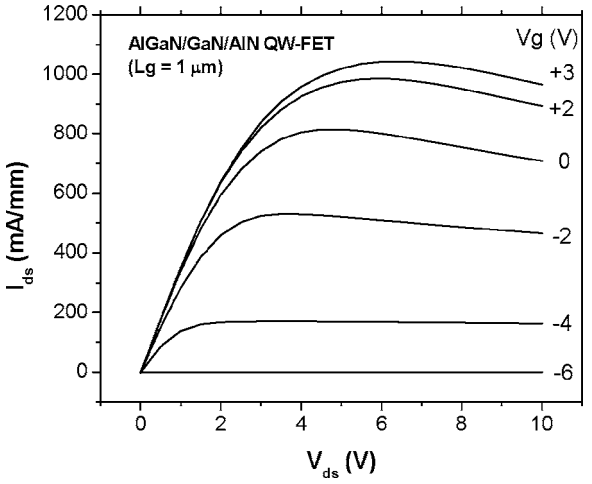

FIG. 3. dc characteristics of fabricated AlGaN/GaN(50 nm)/AlN QW-FETs with 1 μm gate length and 80 μm gate width.

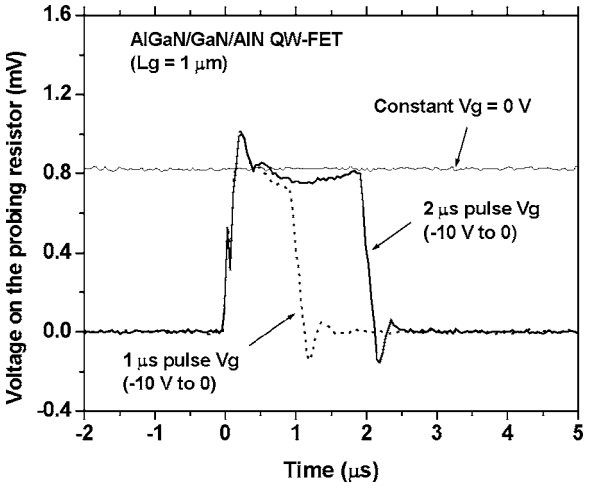

FIG. 4. Gate lag measurement performed for an AlGaN/GaN(50 nm)/AlN QW-FET under pulse gate driving condition. The voltage on the probing resistor is proportional to the drain current. The drain current collapse is calculated by comparing the voltage under pulse driving with that of DC driving. In the measurement, the pulse has a frequency 100 kHz and pulse width 1 μs.

and a 20 nm δ-doped $Al_{0.3}Ga_{0.7}N$ barrier layer with a dopant density of 4.5×10^{12} cm^{-2}. Hall measurement gives 2DEG density n_s of 1.3×10^{13} cm^{-2} and mobility μ of 1400 cm^2 V^{-1} s^{-1}. Devices with a gate length of 1 μm, a source-drain distance of 3 μm, and a gate width of 80 μm are fabricated. The processing starts from the mesa etching by inductive coupled plasma for isolation, and then the ohmic contacts are formed for source and drain by annealing Au/Ti/Al/Ti at 850 °C for 30 s in nitrogen gas. The Schottky gate is Au/Ni bilayer. On-wafer measured drain-source dc current-voltage characteristics of the fabricated AlGaN/GaN/AlN QW-FETs are shown in Fig. 3. The drain current has a maximum value exceeding 1 A/mm and a peak extrinsic transconductance of 180 mS/mm. The device is completely pinched off at a gate bias of −6 V. Compared to one publication[17] reporting the AlGaN/GaN HFET structure with a thin GaN channel grown on bulk AlN substrate, our device shows a much better dc performance.

Even without special passivation processing, the device only exhibits a minor drain current collapse under pulse gate driving. Figure 4 is the gate lag measurement result of an AlGaN/GaN/AlN QW-FET with gate pulsing from −10 V (deep pinch off) to 0 V. For this measurement, a small resistor is connected in series with the FET device, and a digital oscilloscope is used to measure the voltage on this probing resistor, which is proportional to the drain current. Compared with the dc driving, the drain current collapse is small ($<10\%$) under 1 μs gate pulse driving, a dramatic improvement over conventional AlGaN/GaN HFET devices, which generally exhibit a 30%–50% reduction under pulse driving. This result is also comparable to the passivated devices in the literature,[18] which shows the drain current of the Sc_2O_3 passivated Sc_2O_3/AlGaN/GaN HFET device has a decrease of less than 10% in the gate lag measurement.

In summary, we proposed and demonstrated AlGaN/GaN/AlN QW-FET structures. The use of highly resistive AlN epilayer removes the parasitic conduction in the bulk GaN, and the large band edge discontinuity limits the channel electrons spillover, thereby reducing leakage current and drain current collapse. Our simulation results have provided guidance for the device structural optimization. As a result, the fabricated devices show high-level dc performance and small drain current collapse under pulse gate driving.

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